REMARKS/ARGUMENTS

A petition and fee for a two-month extension of time in which to respond is filed contemporaneously herewith.

Claims 1 and 2 were rejected under 35 U.S.C. §103(a) as being obvious and therefore unpatentable because of U.S. patent number 4,292,405 to Ikeda in combination with U.S. patent number 6,839,045 to Ozawa et al. Claims 3 and 4 were objected to as being dependent on a rejected base claim but allowable if re-written to include all limitation of the base claim and any intervening claim.

The applicant submits that claim 1 as amended avoids the art cited by the Examiner and is now in condition for allowance.

In studying the office action, the Examiner admitted that the primary reference of Ikeda does not show the "auxiliary gate lines" limitation. The Examiner then cited Ozawa as teaching the "auxiliary gate lines" limitation.

The Examiner contends that the "cline" shown in FIG. 2 of Ozawa satisfies the auxiliary gate lines limitation and as the claim was originally filed, the Examiner appears to have been correct. Nevertheless, claim 1 as amended avoids the prior art cited by the Examiner because the auxiliary gate line limitation has been amended to recite that the auxiliary gate line is a line having a signal on it, the polarity of which is *opposite* to the polarity of the signal on the (first recited) gate lines. Such a structure is not shown or disclosed in Ozawa.

Using a web browser, the text of the Ozawa reference as published by the U.S. Patent Office through its web site (www.uspot.gov), was searched for occurrences of the term "cline." Although the term was found in several locations within the patent,

"cline" is not described as having a signal on it, the polarity of which is opposite to the "gate" line. In one embodiment, the signal on the "cline" appears to be delayed, but identical to the signal on the "gate" line. Unless the Examiner can identify by column and line number where Ozawa teaches the new limitation added to claim 1, the rejection of the claims must be withdrawn because the subject matter of the amended claim 1 is not found in the prior art.

FIG. 29 shows the "gate" line signal as coming from the output of an inverter, the input of which is coupled to the output of the NAND1 gate. As can be seen in FIG. 29, the output of the NAND1 gate is connected to two inverters. The output of one of these inverters is buffered and thereafter labeled as "cline." Thus, "cline" and "gate1" are identical except for a gate delay caused by the buffer shown in FIG. 29.

Since the references do not show or suggest the structure that is now claimed in claim 1, all of the claims are in condition for allowance. Reconsideration of claims 1-4 is therefore respectfully requested.

Sincerely,

Dated: August 28, 2006

Joseph P. Krause, Reg. No. 32,578
Ladas & Parry
224 South Michigan Avenue
Chicago, Illinois 60604
(312) 427-1300